REMARKS

Claims 1-3 have been examined on their merits, and are all the claims presently pending in the application.

1. Claims 1-3 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Puziol *et al.* (U.S. Patent No. 6,108,777). Applicant respectfully traverses the § 103(a) of claims 1-3 for at least the reasons discussed below.

In the Response dated May 5, 2005, Applicant argued that the present application and Puziol *et al.* solve different problems: the present application is related to a phase binary transmission (PSBT) encoder, while Puziol *et al.* is related to reducing pipeline delays in high performance processors by anticipating taken branches through branch prediction. Thus, there is no suggestion to combine the two references. Applicant also argued that the transparent D flip-flops in the present application and in Puziol *et al.* have different functions: being used as delay elements in the present application, but being used to implement logics in Puziol *et al.* Accordingly, there is no reason for a skilled artisan to pick the transparent D flip-flops from Puziol *et al.* and use them to replace the one-edge triggered D flip-flops in the AAPA.

The Patent Office argues that Puziol *et al.* teach transparent D-type flip-flops having level-sensitive clock inputs and thus reducing the effort required to avoid race conditions (Puziol *et al.*, col. 6, lines 42-53). However, Applicant submits that this teaching does not provide motivation or suggestion to combine Puziol *et al.* and the AAPA.

Fig. 2 of the present application shows prior art circuitry for phase shifted binary transmission encoding, using an exclusive or gate XOR with feedback. A one-edge triggered D flip-flop is used in the feedback circuit to provide a one-bit length delay. However, to be used in a fast phase shifted binary transmission, the circuit using the one-edge triggered D flip-flop is either too inexact or too slow (Specification, page 4, the second full paragraph).

Neither the AAPA nor Puziol *et al.* teaches or suggests that a device having level sensitive clock inputs can help to solve the problem of the AAPA. Thus, although Puziol *et al.* mention that a transparent D flip-flop have level sensitive clock inputs, there is no suggestion or motivation to pick the transparent D flip-flop in Puziol *et al.* and use it to replace one-edge triggered D flip-flop shown in Fig. 2 of the present application.

In addition, Puziol *et al.* mention that its two-phase design reduces the effort required to avoid race conditions. However, the effort required to avoid race conditions is not a problem of the AAPA and is irrelevant to the problem of the AAPA. Neither the AAPA nor Puziol *et al.* teaches or suggests that reducing the effort required to avoid race conditions can help to solve the problem of the AAPA. There is no reason for a skilled artisan, facing the problem of the AAPA, to pick the transparent D flip-flop used in Puziol *et al.* for reducing the effort required to avoid race conditions and use it to replace the one-edge triggered D flip-flop of the AAPA.

Facing the problem of the AAPA, skilled artisans would have many possible approaches to improve the speed and accuracy of the phase shifted binary transmission encoding. Replacing the one-edge triggered D flip-flop with a transparent D flip-flop is only one of them. It is

Applicant who found that a transparent D flip-flop can help to improve the speed and accuracy of the AAPA.

It is true that one difference between the claimed invention and the AAPA is that the AAPA uses one-edge triggered D flip-flops, while the claimed invention uses transparent D flip-flops. It is also true that Puziol *et al.* use transparent D flip-flops in its circuit. However, as Applicant argued before, the transparent D flip-flops in Puziol *et al.* are for implementing logic, while the problem of the AAPA is that the circuits are either too inexact or too slow. Given the different purposes of Puziol *et al.* and the present application, the different problems solved by Puziol *et al.* and the present application, and the different usages of the transparent D flip-flops in Puziol *et al.* and the claimed invention, there is simply no reason or suggestion for a skilled artisan to pick the transparent D flip-flops in Puziol *et al.* and use them to replace the one-edge triggered D flip-flops of the AAPA.

The Patent Office argues that a reconstruction is proper so long as it does not include knowledge gleaned only from the applicant's disclosure. However, to pick the transparent D flip-flop used in Puziol *et al.* for implementing logic and add it to the AAPA, which needs improved speed and accuracy, is exactly the collection of portions of the claimed invention from references that are irrelevant to each other and putting the collected portions together to reconstruct the claimed invention.

Furthermore, the combination of AAPA and Puziol *et al.* fails to teach or suggest at least the features of the read-in pulse, as recited in claim 1. As discussed in the instant specification, the delay created by the exclusive OR gate/flip-flop combination in the prior art circuit causes a

one-bit delay in the prior art encoding circuit, which is unacceptable for high bit rate encoding. While Puziol *et al.* discloses the transparent D flip-flop, there is no discussion of relationships between the read-in pulse, the data input and the delay time of a delay element. The combination of AAPA and Puziol *et al.* fails to teach or suggest any relationship between the read-in pulse, the data input and the delay time of a delay element as well.

Based on at least the foregoing reasons, Applicant submits that independent claim 1 is allowable over the combination of AAPA and Puziol *et al.*, and further submits that claims 2 and 3 are allowable as well, at least by virtue of their dependency from claim 1. Applicant respectfully requests that the Patent Office reconsider and withdraw § 103(a) of claims 1-3.

2. Claims 1-3 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over AAPA in view of Kojima *et al.* (U.S. Patent Publication No. 2002/0196064). Applicant respectfully traverses the § 103(a) of claims 1-3 for at least the reasons discussed below.

In the Response dated May 5, 2005, Applicant argued that Kojima *et al.* have nothing to do with the PSBT encoder of the present application, and given the different problems solved by the present application and Kojima *et al.*, there is no suggestion or motivation for a skilled artisan to combine the references.

The Patent Office has argued that Kojima *et al.* discloses, *inter alia*, transparent D-type flip-flops providing a fast performance and low power consumption. However, Kojima *et al.* only mention that a hybrid-latch flip-flop (HLFF) has fast performance and relatively low power

consumption (Kojima, paragraph 0003). Kojima *et al.* do not indicate whether the HLFF is transparent or not. The Patent Office's interpretation of Kojima *et al.* is mistaken.

In addition, as shown in Fig. 1 of Kojima *et al.*, the HLFF has differential outputs Q122 and Q_N 121. However, in the AAPA, each of FF1 and FF2 has only one output. Thus, there is no reason for a skilled artisan to pick the HLEF in Kojima *et al.* and use it to replace the one-edge triggered D flip-flop in the AAPA. Even if a skilled artisan were to combine Kojima *et al.* with the AAPA, the combination would not result in the claimed invention.

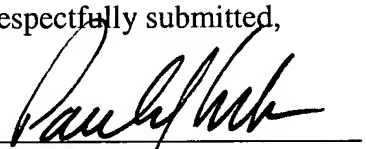
Furthermore, the combination of AAPA and Kojima *et al.* fails to teach or suggest at least the features of the read-in pulse, as recited in claim 1. As discussed in the instant specification, the delay created by the exclusive OR gate/flip-flop combination in the prior art circuit causes a one-bit delay in the prior art encoding circuit, which is unacceptable for high bit rate encoding. There is no discussion in Kojima *et al.* of relationships between the read-in pulse, the data input and the delay time of a delay element. The combination of AAPA and Kojima *et al.* fails to teach or suggest any relationship between the read-in pulse, the data input and the delay time of a delay element as well.

Based on at least the foregoing reasons, Applicant submits that independent claim 1 is allowable over the combination of AAPA and Kojima *et al.*, and further submits that claims 2 and 3 are allowable as well, at least by virtue of their dependency from claim 1. Applicant respectfully requests that the Patent Office reconsider and withdraw § 103(a) of claims 1-3.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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